**Amendment to the Claims:**

This listing of claims will replace all prior versions and listings of claims in the application.

**Listing of Claims:**

1. (Currently Amended) A method, comprising:

receiving a media clock signal;

creating a capture pulse **with asynchronous logic** to synchronize the media clock signal with a memory clock signal;

capturing media data at a transition of the capture pulse; and

storing the media data in a synchronous memory.

2. (Previously Presented) The method of claim 1 further comprising scheduling to store the media data in the synchronous memory.

3. (Previously Presented) The method of claim 2 wherein scheduling to store the media data comprises initiating a signal based upon a capture pulse.

4. (Previously Presented) The method of claim 1 further comprising multiplexing to store the media data in the synchronous memory.

5. (Previously Presented) The method of claim 4 wherein multiplexing to store the media data comprises receiving a write select signal to store the media data.

6. (Previously Presented) The method of claim 1 wherein said receiving a media clock signal comprises receiving a clock signal of a queue comprising data to capture.

7. (Canceled)

8. (Previously Presented) The method of claim 1 wherein said creating a capture pulse to synchronize the media clock signal comprises creating a capture pulse to synchronize the media clock signal with a transition of the memory clock signal.

9. (Previously Presented) The method of claim 1 wherein said capturing data at a transition of the capture pulse comprises capturing data from a queue.

10. (Previously Presented) The method of claim 1 wherein said storing the data in a synchronous memory comprises writing a memory word to the synchronous memory.

11.(Currently Amended) An apparatus, comprising:

a synchronizer **including an asynchronous state machine**; ~~and~~

a buffer coupled to said synchronizer; and

a synchronous memory coupled to said buffer.

12. (Previously Presented) The apparatus of claim 11, further comprising a multiplexer coupled to more than one buffer.

13. (Previously Presented) The apparatus of claim 11, further comprising a scheduler coupled to said synchronous memory.

14. (Previously Presented) The apparatus of claim 11, further comprising an inbound register coupled to said buffer.

15. (Canceled)

16. (Previously Presented) The apparatus of claim 11, wherein said buffer comprises a buffer to capture data from an inbound register.

17. (Previously Presented) The apparatus of claim 11, wherein said synchronous memory comprises a synchronous random access memory.

18. (Previously Presented) The apparatus of claim 11, wherein said synchronous memory comprises memory to store data from an inbound register.

19. – 23. (Canceled)

24. (Currently Amended) A machine-readable medium containing instructions, which when executed by a machine, cause said machine to perform operations, comprising:

receiving a media clock signal;

creating a capture pulse **with asynchronous logic** to synchronize the media clock signal with a memory clock signal;

capturing media data at a transition of the capture pulse; and

storing the media data in a synchronous memory.

25. (Previously Presented) The machine-readable medium of claim 24 further comprising scheduling to store the media data in the synchronous memory.

26. (Previously Presented) The machine-readable medium of claim 24 further comprising multiplexing to store the media data in the synchronous memory.

27. (Canceled)

28. (Previously Presented) The machine-readable medium of claim 24 wherein said creating a capture pulse to synchronize the media clock signal comprises creating a capture pulse to synchronize the media clock signal with a transition of the memory clock signal.

29. (Previously Presented) The machine-readable medium of claim 24 wherein said capturing data at a transition of the capture pulse comprises capturing data from a queue.

30. (Previously Presented) The machine-readable medium of claim 24 wherein said storing the data in a synchronous memory comprises writing a memory word to the synchronous memory.